

00E #036/

APPARATUS FOR DECODING RECEIVING SIGNAL

BACKGROUND OF THE INVENTION

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FIELD OF THE INVENTION

The present invention generally relates to digital communications, and more particularly, to an apparatus for decoding encoded voice signal.

This application is a counterpart of Japanese patent application, Serial Number 32588/2001, filed February 8, 2001, the subject matter of which is incorporated herein by reference.

TOGETHER WITH THE DRAWINGS

DESCRIPTION OF THE RELATED ART

Pulse code modulation (PCM) code is one of the codes which modulate an analog voice signal to a digital data. PCM code is sampled the analog voice signal every a certain timing as a digital data and is stored one. The quality of the digital data depends on the number of sampling per second (sampling frequency) and the number of bits of the data (sample quantizing level). For example, the standard systems, the Cordless Telephone II(CT2), specify sampling at 8 kHz and quantizing to 15 levels. Adaptive differential pulse code modulation (ADPCM)

code also is sampled the voice signal every a certain timing as a digital data, such as PCM code. However, ADPCM code is produced by using both the present digital data and the prior sampled digital data. ADPCM saves memory capacity for storing the digital data in comparison with PCM.

5 In the cordless telephone systems, an ADPCM data (ADPCM signal) which is modulated from a PCM data (PCM signal) using an ADPCM encoder, has occasionally transmission errors when a distance between a cordless telephone and a network station is long or when the cordless telephone receives interference from another systems. When the transmitted ADPCM data which has transmission errors is decoded and reproduced as a voice, the reproduced voice has noise. As one method of solving this problem, in time division multiple access (TDMA) systems, the decoding apparatus does not reproduce the ADPCM data with transmission errors as a voice when a synchronous pattern (a unique word) is not detected. According to this method, all ADPCM data with
15 transmission errors is not reproduced. This causes a dumb state in a telephone conversation. Therefore, in the conventional decoding apparatus, the more the ADPCM data has transmission errors, the more a dumb state increases in order to control noise. Thus, since a telephone conversation becomes fragmentary condition and the quality of a telephone conversation becomes lower.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an apparatus for decoding receiving signal that may improve the quality of a telephone conversation even if ADPCM data has transmission errors.

5 According to one aspect of the present invention, for achieving the above object, there is provided an apparatus for decoding receiving encoded voice data, is provided with a demodulator which demodulates the encoded voice data and provides a demodulated encoded voice data, an adaptive differential pulse code modulation decoder which decodes the demodulated encoded voice data and
10 provides a pulse code modulation data, an error detector which detects whether error is present in the encoded voice data and outputs a detection result and a limiter which outputs either the pulse code modulation data or a predetermined value in accordance with the detection result.

The above and further objects and novel features of the invention will more
15 fully appear from the following detailed description, appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a decoding apparatus according to a first
20 preferred embodiment of the present invention.

Fig. 2 is a block diagram showing a first limiter portion being used in a first, a second or a third preferred embodiments of the present invention.

Fig. 3 is a block diagram showing a second limiter portion being used in a first, a second or a third preferred embodiments of the present invention.

5 Fig. 4 is a block diagram showing a third limiter portion being used in a first, a second or a third preferred embodiments of the present invention.

Fig. 5 is a wave form chart output by a decoding apparatus according to a first preferred embodiment of the present invention.

10 Fig. 6 is a block diagram showing a decoding apparatus according to a second preferred embodiment of the present invention.

Fig. 7 is a block diagram showing a first threshold value setting portion being used in a second or a fourth preferred embodiments of the present invention.

Fig. 8 is a timing chart showing the operation of the first threshold value setting portion.

15 Fig. 9 is a wave form chart output by a decoding apparatus according to a second preferred embodiment of the present invention.

Fig. 10 is a block diagram showing a decoding apparatus according to a third preferred embodiment of the present invention.

20 Fig. 11 is a block diagram showing a second threshold value setting portion being used in a third preferred embodiment of the present invention.

Fig. 12 is a timing chart showing the operation of the second threshold value setting portion.

Fig. 13 is a wave form chart output by a decoding apparatus according to a third preferred embodiment of the present invention.

Fig. 14 is a block diagram showing a decoding apparatus according to a fourth preferred embodiment of the present invention.

Fig. 15 is a block diagram showing a fourth limiter portion being used in a fourth preferred embodiment of the present invention.

Fig. 16 is a block diagram showing a fifth limiter portion being used in a fourth preferred embodiment of the present invention.

Fig. 17 is a block diagram showing a sixth limiter portion being used in a fourth preferred embodiment of the present invention.

Fig. 18 is a wave form chart output by a decoding apparatus according to a fourth preferred embodiment of the present invention.

Fig. 19 is the structure of a burst signal used by the embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In what follows, the present invention will be explained with embodiments of the present invention. However, the invention is not limited to the specific

embodiments. Moreover, not all the combinations of the characteristics of the present invention described in the embodiments are essential to the problem solving means by the present invention.

First, a burst signal (radio signal) which is received by a decoding apparatus
5 for TDMA systems at every certain timing will be described with Fig. 19. As shown in Fig. 19(a), the burst signal t_1, t_2, \dots is received at every 5 msec (millisecond) in the talking mode or at every an integer times of 5 msec in the waiting mode. Each burst signal t_1, t_2, \dots comprises a frame which has 625 μ sec (microsecond) in length. As shown in Fig. 19(b), the frame has a preamble
10 portion, a synchronous pattern portion followed by the preamble portion, a message data portion followed by the synchronous pattern portion and a CRC (cyclic redundancy check) data portion followed by the message data portion. In addition, the frame has a control data portion et al such as guard bits.

The preamble portion stores phase information (information for locking initial
15 phase) which is used for right capturing the burst signal transmitted by a transmitter. The synchronous pattern portion stores synchronous pattern information that is used for detecting synchronism of the burst signal at a receiver. A detecting synchronism is called as aquisition. The message data portion stores voice information. The CRC portion is data portion for detecting error and stores
20 an error correcting code information that is used for detecting or correcting an error

in the burst signal.

The decoding apparatus is capable of being provided in the transmitter or the receiver.

(First Preferred Embodiment)

5 A decoding apparatus for decoding encoded voice signal according to a first preferred embodiment of the present invention will be described with reference to Figs. 1-5. Fig. 1 is a block diagram showing the structure of the decoding apparatus having a limiter portion. Figs. 2-4 are block diagrams showing the structure of the limiter portions of the decoding apparatus. Fig. 5 shows a wave
10 form chart output by the decoding apparatus according to the first preferred embodiment of the present invention.

First, the structure and operation of the decoding apparatus according to the first preferred embodiment of the present invention will be described. The decoding apparatus according to the first preferred embodiment of the present
15 invention comprises a demodulator 101, an ADPCM decoder 102, an error detector 103, a limiter 104 and a PCM decoder 105.

The demodulator 101 locks a phase of the received burst signal in accordance with phase information stored in the preamble portion of a radio signal (the received burst signal) RF. The demodulator 101 demodulates voice
20 information which is stored in the message data portion and error correcting code

information which is stored in the CRC data portion, and outputs ADPCM format data (ADPCM signal) APO and demodulated data (demodulated signal) RD.

The ADPCM decoder 102 decodes the ADPCM format data APO and outputs PCM format data (PCM signal) PO.

5 The error detector 103 detects whether the radio signal RF has a transmission error in accordance with an error data in the demodulated data RD. When the error is detected, the error detector 103 outputs a detection result (a detection signal) CRCERR which has a supply voltage level ('H' level). On the other hand, when the error is not detected, the error detector 103 outputs the detection result CRCERR which has a ground voltage level ('L' level).

10 The limiter 104 has a limit value. The limiter 104 outputs either the PCM format data PO or the limit value as a PCM format data POL in accordance with the voltage level of the detection result CRCERR. The limiter 104 will be described later in detail.

15 The PCM decoder 105 decodes the PCM format data POL and outputs an analog voice data (analog voice signal) AVD.

The limiter 104 will be described with reference to Figs. 2-4. Fig. 2 shows a first limiter, Fig. 3 shows a second limiter and Fig. 4 shows a third limiter.

20 First, the first limiter 104 will be described with Fig. 2 as follows. The first limiter 104 comprises a comparator 201, a comparator 202 and an output portion

detection result CRCERR and the comparison result GT are 'H' level, the logic product 203A outputs a logic product result 203a which has 'H' level. On the other hand, when the voltage level of the detection result CRCERR or the comparison result GT is 'L' level, the logic product 203A outputs the logic product result 203a which has 'L' level.

The logic product 203B operates a logic product between the detection result CRCERR and the comparison result LT. When both of the voltage level of the detection result CRCERR and the comparison result LT are 'H' level, the logic product 203B outputs a logic product result 203b which has 'H' level. On the other hand, when the voltage level of the detection result CRCERR or the comparison result LT is 'L' level, the logic product 203B outputs the logic product result 203b which has 'L' level.

The selector 203C outputs the upper limit value as the PCM format data POL when the logic product result 203a has 'H' level and the lower limit value as the PCM format data POL when the logic product result 203b has 'H' level. Furthermore, the selector 203C outputs the PCM format data PO as the PCM format data POL when both the logic product result 203a and the logic product result 203b have 'L' level.

According to the first limiter 104, the upper limit value and the lower limit value can be set up, individually and freely. Therefore, the user can obtain the

analog voice signal which has a desired band.

Next, the second limiter 104 will be described with Fig. 3 as follows. The second limiter 104 comprises a numerical value data selector 301, a code data selector 302, a comparator 303 and an output portion 304. The output portion 304 comprises a logic product (AND gate) 304A, a selector 304B and a code combiner 304C. The second limiter 104 has an upper limit value of which format is the absolute value. The upper limit value is the greatest common absolute value between the absolute value of the largest amplitude value of a voice signal and the absolute value of the smallest amplitude value of a voice signal. Even if the voice signal having the level of the largest amplitude value is reproduced, the reproduced voice signal does not have noise. Even if the voice signal having the level of the smallest amplitude value is reproduced, the reproduced voice signal does not have noise. For example, when the largest amplitude value of the voice signal is +12 (plus 12) and when the smallest amplitude value is -10 (minus 10), the upper limit value X which satisfies an expression $|+12| \geq X$ and $|-10| \geq X$ is 10 ($X=10$). In this case, the upper limit value is '10'.

The numerical value data selector 301 selects a numerical value data of the PCM format data PO. For example, when the PCM format data PO comprises 4 bits, the most significant bit (MSB) indicates the code data and the other 3 bits except for the MSB indicate the numerical value data. The numerical value data

selector 301 selects 3 bits except for the MSB as the numerical value data.

The code data selector 302 selects a code data of the PCM format data PO.
In the above case, the code data selector 302 selects the MSB as the code data.

The comparator 303 compares the upper limit value of which format is the
5 absolute value and the numerical value data of the PCM format data PO. When
the numerical value data is larger than the upper limit value, the comparator 303
outputs a comparison result GT which has 'H' level. On the other hand, when the
numerical value data is smaller than the upper limit value, the comparator 303
outputs a comparison result GT which has 'L' level.

The logic product 304A operates a logic product between the detection result
10 CRCERR and the comparison result GT. When both of the voltage level of the
detection result CRCERR and the comparison result GT are 'H' level, the logic
product 304A outputs a logic product result 304a which has 'H' level. On the
other hand, when the voltage level of the detection result CRCERR or the
15 comparison result GT is 'L' level, the logic product 304A outputs the logic product
result 304a which has 'L' level.

The selector 304B selects the upper limit value when the logic product result
304a has 'H' level and outputs one as a selection result 304b. Furthermore, the
selector 304B selects the numerical value data of the PCM format data PO when
20 the logic product result 304a has 'L' level and outputs one as a selection result

304b.

The code combiner 304C combines the selection result 304b with the code data of the PCM format data PO and outputs one as the PCM format data POL. By the way, the number of bits of the upper limit data is the same as the number of bits of the numerical value data of the PCM format data PO. For example, the numerical value data of the PCM format data PO and the upper limit data comprise 3 bits. In the above case, the code combiner 304C adds the code data of the PCM format data PO which comprises one-bit to the front position of the most significant bit of the selection result signal 304b. The number of bits of the PCM format data POL becomes 4 bits.

According to the second limiter 104, the upper limit value and the lower limit value of the first limiter can be combined as one limit value. Therefore, the second limiter 104 can save the capacitance of the memory which stores the limit value.

Next, the third limiter 104 will be described with Fig. 4 as follows. The third limiter 104 comprises a numerical value data selector 301, a code data selector 302, a comparator 303 and an output portion 401. The output portion 401 comprises a logic product (AND gate) 304A, a code combiner 401A and a selector 401B. An upper limit value used in the third limiter 104 is the same as the upper limit value used in the second limiter 104.

The code combiner 401A combines the upper limit value with the code data of the PCM format data PO and outputs combined data 401a.

The selector 401B selects the combined data 401a when the logic product result 304a has 'H' level and outputs one as the PCM format data POL.

5 Furthermore, the selector 401B selects the original PCM format data PO when the logic product result 304a has 'L' level and outputs one as the PCM format data POL.

According to the third limiter 104, the original PCM format data PO can be output as the PCM format data POL. Therefore, the third limiter 104 can save the time and power dissipation to combine the numerical value data of the PCM format data PO with the code data again.

Next, the operation of the decoding apparatus with the first limiter 104 according to the first preferred embodiment of the present invention will be described with Fig. 5 as follows. As shown in Fig. 5, the decoding apparatus
15 according the first preferred embodiment demodulates the receive signals at timing t1, t2, t3, t4,... In this case, the demodulation signal RD at timing t2 has transmission errors. In timing t2, the voltage level of the detection result CRCERR is 'H' level.

Until the point 501 from the point 500, the amplitude value of the PCM format data PO decoded by the ADPCM decoder 102, is lower than the upper limit value
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and higher than the lower limit value. The limiter 104 outputs the PCM format data PO as the PCM format data POL. Therefore, the PCM decoder 105 decodes the PCM format data PO and outputs the decoded PCM format data PO as the analog voice data AVD.

5 At the point 501, the PCM format data PO is lower than the lower limit value. The limiter 104 outputs the lower limit value as the PCM format data POL. Therefore, the PCM decoder 105 does not decode the PCM format data PO but the lower limit value, and outputs the decoded lower limit value as the analog voice data AVD.

10 Until the point 502 from the point 501, the PCM format data PO is lower than the upper limit value and higher than the lower limit value. Therefore, the PCM decoder 105 decodes the PCM format data PO and outputs the decoded PCM format data PO as the analog voice data AVD.

15 At the point 502, the PCM format data PO is higher than the upper limit value. The limiter 104 outputs the upper limit value as the PCM format data POL. Therefore, the PCM decoder 105 does not decode the PCM format data PO but the upper limit value, and outputs the decoded upper limit value as the analog voice data AVD. Since then, the decoding apparatus conducts the same operation described the above.

20 The decoding apparatus according to the first preferred embodiment of the

present invention has the following effect.

The decoding apparatus according to the first preferred embodiment of the present invention reproduces the limit data (upper limit value or lower limit value) when the receive signal has transmission errors. The decoding apparatus according to the first preferred embodiment can avoid a dumb state in comparison with the conventional decoding apparatus. Therefore, the decoding apparatus according to the first preferred embodiment can be good the quality of a telephone conversation.

(Second Preferred Embodiment)

A decoding apparatus for decoding encoded voice signal according to a second preferred embodiment of the present invention will be described with reference to Figs. 6-9. Fig. 6 is a block diagram showing the structure of the decoding apparatus. Fig. 7 is a block diagram showing the structure of a threshold value setting portion of the decoding apparatus. Fig. 8 is a timing chart showing the operation of the threshold value setting portion of the decoding apparatus. Fig. 9 shows a wave form chart output by the decoding apparatus according to the second preferred embodiment of the present invention. Like elements are given like or corresponding reference numerals in the first preferred embodiment. Thus, dual explanations of the same elements are avoided.

First, the structure and operation of the decoding apparatus according to the

second preferred embodiment of the present invention will be described. The decoding apparatus according to the second preferred embodiment of the present invention comprises a demodulator 101, an ADPCM decoder 102, an error detector 103, a limiter 104, a PCM decoder 105 and a threshold value setting
5 portion 601.

The threshold value setting portion 601 calculates the average value of the amplitude value of the PCM format data PO output by the ADPCM decoder 102. The threshold value setting portion 601 outputs the calculated average value as the limit value THV. The moving average method is used as the method for
10 calculating the average value.

Next, the structure and the operation of the threshold value setting portion 601 will be described with Figs. 7-8 as follows. The threshold value setting portion 601 comprises a numerical value data selector 301, an average calculating portion 701 and a latch portion 702. The average calculating portion 701
15 comprises an accumulator 701A and a multiple portion 701B.

The accumulator 701A conducts the accumulating operation which is to add the numerical value data of the PCM format data PO and the sum of the numerical value data which is calculated before and to store the addition result ACCO. As shown in Fig. 8, the accumulator 701A receives a one-shot pulse signal ARESET
20 which has 'H' level when the accumulator 701A conducts the accumulating

operation at N times (N is a positive number). At this time, the accumulator 701A resets the addition result ACCO which has been stored. The accumulator 701A can output the addition result ACCO either at every each accumulating operation or at every N times in accordance with the calculating method which is applied in the multiple portion 701B.

The multiple portion 701B executes the multiplication operation of the addition result ACCO and a coefficient and obtains the average value 701b. When the accumulator 701A outputs the addition result ACCO at every N times, the multiple portion 701B can obtain the average value 701b by dividing N into the addition result ACCO. When the coefficient is one the nth power of second, the multiple portion 701B can comprise a shift resistor circuit. It goes without saying that an adder can be used instead of the multiple portion 702A to calculate the average value.

The latch portion 702 stores a new average value 701b when a control signal DLT which is a one-shot pulse signal having 'H' level is input (see Fig. 8). The latch portion 702 outputs the stored new average value 701b as the limit value. When the control signal DLT which has 'L' level is input, the latch portion 702 does not store the new average value 701b and outputs the storing old average value 701b as the limit value.

Next, the operation of the decoding apparatus according to the second

preferred embodiment of the present invention will be described with Fig. 9 as follows. As shown in Fig. 9, the decoding apparatus according the second preferred embodiment receives the receive signals at timing t1, t2, t3, t4,... In this case, the demodulation signal RD at timing t2 has transmission errors. In
5 timing t2, the voltage level of the detection result CRCERR is 'H' level.

Until the point 901 from the point 900, the amplitude value of the PCM format data PO decoded by the ADPCM decoder 102, is lower than the upper limit value and higher than the lower limit value. The limiter 104 outputs the PCM format data PO as the PCM format data POL. Therefore, the PCM decoder 105
10 decodes the PCM format data PO and outputs the decoded PCM format data as the analog voice data AVD.

At the point 901, the PCM format data PO is lower than the lower limit value. The limiter 104 outputs the lower limit value as the PCM format data POL. Therefore, the PCM decoder 105 does not decode the PCM format data PO but
15 the lower limit value, and outputs the decoded lower limit value as the analog voice data AVD. The limit value at this time is the average value which is calculated in the threshold value setting portion 601 based on N data of the PCM format data PO before the point 901. For example, when the average value is 10, the upper limit value is +10 (plus 10) and the lower limit value is -10 (minus 10).

20 Until the point 902 from the point 901, the PCM format data PO is lower than

the upper limit value and higher than the lower limit value. Therefore, the PCM decoder 105 decodes the PCM format data PO and outputs the decoded PCM format data PO as the analog voice data AVD.

At the point 902, the PCM format data PO is higher than the upper limit value.

5 The limiter 104 outputs the upper limit value as the PCM format data POL.

Therefore, the PCM decoder 105 does not decode the PCM format data PO but the upper limit value, and outputs the decoded upper limit value as the analog voice data AVD. The limit value at this time is the average value which is calculated in the threshold value setting portion 601 based on N data of the PCM format data PO before the point 902. In the second embodiment of the present invention, the limit value is calculated at the two points 901 and 902 and the different limit value are applied. Therefore, it often happens that the different limit value are applied at each point. Since then, the decoding apparatus conducts the same operation described the above.

15 The decoding apparatus according to the second preferred embodiment of the present invention can have the same effects being described in the first preferred embodiments of the present invention.

Furthermore, the decoding apparatus according to the second preferred embodiment of the present invention can have the following effect.

20 The decoding apparatus according to the second preferred embodiment of

the present invention does not apply the fixed data as the limit value but the no-
fixed data which is the average value of the PCM format data PO just before the
PCM format data PO exceeds the upper or lower limit data. Therefore, when the
receive signal has transmission errors, the decoding apparatus according to the
5 second preferred embodiment can reproduce the voice signal based on an
amplitude range of the receive signal continuing just before the receive signal
which has transmission errors. Therefore, the decoding apparatus according to
the second preferred embodiment can be good the quality of a telephone
conversation.

(Third Embodiment)

A decoding apparatus for decoding encoded voice signal according to a third
preferred embodiment of the present invention will be described with reference to
Figs. 10-13. Fig. 10 is a block diagram showing the structure of the decoding
apparatus. Fig. 11 is a block diagram showing the structure of a threshold value
15 setting portion of the decoding apparatus. Fig. 12 is a timing chart showing the
operation of the threshold value setting portion of the decoding apparatus. Fig.
13 shows a wave form chart output by the decoding apparatus according to the
third preferred embodiment of the present invention. Like elements are given like
or corresponding reference numerals in the first or second preferred embodiments.

20 Thus, dual explanations of the same elements are avoided.

First, the structure and operation of the decoding apparatus according to the third preferred embodiment of the present invention will be described. The decoding apparatus according to the third preferred embodiment of the present invention comprises a demodulator 101, an ADPCM decoder 102, an error
5 detector 103, a limiter 104, a PCM decoder 105 and a threshold value setting portion 1001.

The threshold value setting portion 1001 calculates the average value of the absolute value of the amplitude value of the PCM format data PO. The threshold value setting portion 1001 outputs the calculated average value as the limit value THV. The threshold value setting portion 1001 does not use the absolute value of
10 the amplitude value of the PCM format data PO which has transmission errors, in order to calculate the average value.

Next, the structure and the operation of the threshold value setting portion 1001 will be described with Figs. 11-12 as follows. The threshold value setting
15 portion 1001 comprises a numerical value data selector 301, an average calculating portion 701, and an output portion 1102. The output portion 1102 comprises a logic product (AND gate) 1102A, a latch portion 1102B and an inverter 1102C.

The logic product 1102A operates a logic product between the detection
20 result CRCERR which is inverted by the inverter 1102C and the control signal DLT.

When both of the voltage level of the inverted detection result CRCERR and the control signal DLT are 'H' level, the logic product 1102A outputs a logic product result 1102a which has 'H' level (see Fig. 12). On the other hand, when the voltage level of the inverted detection result CRCERR or the control signal DLT is 'L' level, the logic product 1102A outputs the logic product result 1102a which has 'L' level (see Fig. 12).

The latch portion 1102B stores a new average value 701b when the logic product result 1102a which is a one-shot pulse signal having 'H' level is input (see Fig. 12). The latch portion 1102B outputs the stored new average value 701b as the limit value. When the logic product result 1102a which has 'L' level is input, the latch portion 1102B does not store the new average value 701b and outputs the storing old average value 701b as the limit value. Therefore, the latch portion 1102B does not use the absolute value of the amplitude value of the PCM format data PO which has transmission errors, in order to calculate the average value.

Next, the operation of the decoding apparatus according to the third preferred embodiment of the present invention will be described with Fig. 13 as follows. As shown in Fig. 13, the decoding apparatus according the third preferred embodiment receives the receive signals at timing t1, t2, t3, t4,... In this case, the demodulation signal RD at timing t1 does not have transmission errors and the demodulation signal RD at timing t2 has transmission errors. In

timing t2, the voltage level of the detection result CRCERR is 'H' level.

Until the point 1302 from the point 1301, the amplitude value of the PCM format data PO decoded by the ADPCM decoder 102, is lower than the upper limit value and higher than the lower limit value. The limiter 104 outputs the PCM format data PO as the PCM format data POL. Therefore, the PCM decoder 105 decodes the PCM format data PO and outputs the decoded PCM format data PO as the analog voice data AVD.

At the point 1302, the PCM format data PO is lower than the lower limit value. The limiter 104 outputs the lower limit value as the PCM format data POL. Therefore, the PCM decoder 105 does not decode the PCM format data PO but the lower limit value, and outputs the decoded lower limit value as the analog voice data AVD. The limit value at this time is the average value which is calculated in the threshold value setting portion 1001 based on N data (A) of the PCM format data PO at timing t1. In other words, N data of the PCM format data PO at timing t2 is not used to calculate the average value. For example, when the average value is 10, the upper limit value is +10 (plus 10) and the lower limit value is -10 (minus 10).

Until the point 1303 from the point 1302, the PCM format data PO is lower than the upper limit value and higher than the lower limit value. Therefore, the PCM decoder 105 decodes the PCM format data PO and outputs the decoded

PCM format data PO as the analog voice data AVD.

At the point 1303, the PCM format data PO is higher than the upper limit value. The limiter 104 outputs the upper limit value as the PCM format data POL. Therefore, the PCM decoder 105 does not decode the PCM format data PO but
5 the upper limit value, and outputs the decoded upper limit value as the analog voice data AVD. The limit value at this time is the average value which is calculated based on N data (A) of the PCM format data PO at timing t1. Since then, the decoding apparatus conducts the same operation described the above.

The decoding apparatus according to the third preferred embodiment of the present invention can have the same effects being described in the first and
10 second preferred embodiments of the present invention.

Furthermore, the decoding apparatus according to the third preferred embodiment of the present invention can have the following effect.

The decoding apparatus according to the third preferred embodiment of the present invention does not apply the average value of the absolute value of the
15 PCM format data PO which has transmission errors, but the average value of the absolute value of the PCM format data PO which does not have transmission errors. The decoding apparatus according to the third preferred embodiment can reproduce the voice signal based on the just before receive signal which does not
20 have transmission errors. Therefore, the decoding apparatus according to the

third preferred embodiment can be good the quality of a telephone conversation.

(Fourth Embodiment)

A decoding apparatus for decoding encoded voice signal according to a fourth preferred embodiment of the present invention will be described with reference to Figs. 14-18. Fig. 14 is a block diagram showing the structure of the decoding apparatus having a limiter portion. Figs. 15-17 are block diagrams showing the structure of the limiter portions of the decoding apparatus. Fig. 18 shows a wave form chart output by the decoding apparatus according to the fourth preferred embodiment of the present invention. Like elements are given like or corresponding reference numerals in the first, second or third preferred embodiments. Thus, dual explanations of the same elements are avoided.

First, the structure and operation of the decoding apparatus according to the fourth preferred embodiment of the present invention will be described. The decoding apparatus according to the fourth preferred embodiment of the present invention comprises a demodulator 101, an ADPCM decoder 102, an error detector 103, a PCM decoder 105, a threshold value setting portion 601, a counter 1401 and a limiter 1402.

The counter 1401 inputs the PCM format data PO which is output by the ADPCM decoder 102 and the limit value THV which is output by the threshold value setting portion 601. The counter 1401 counts the number of times that the

PCM format data PO is over the limit value THV. The counter 1401 outputs a count result COUNT which has 'H' level, when the counted value is over the predetermined value.

The limiter 1402 has a limit value. The limiter 1402 outputs either the PCM format data PO or the limit value as a PCM format data POL in accordance with the voltage level of the detection result CRCERR. In addition, the limiter 1402 conducts either outputting the PCM format data POL of which value is very small or stopping outputting the PCM format data POL, when the count result COUNT is input. The limiter 1402 will be described with reference to Figs. 15-17 in detail.

First, the fourth limiter 1402 will be described with Fig. 15 as follows. The fourth limiter 1402 comprises a comparator 201, a comparator 202 and an output portion 1501. The output portion 1501 comprises a logic product (AND gate) 203A, a logic product 203B, a selector 203C and a controller 1501A. The fourth limiter 1402 has an upper limit value and a lower limit value. The user can freely set the upper limit value and the lower limit value. For example, the user can set the upper limit value which is calculated by the threshold value setting portion 601 and the lower limit value which is the reversed upper limit value.

The selector 203C outputs the upper limit value as a selected data 203c when the logic product result 203a has 'H' level and the lower limit value as the selected data 203c when the logic product result 203b has 'H' level. Furthermore,

the selector 203C outputs the PCM format data PO as the selected data 203c when both the logic product result 203a and the logic product result 203b has 'L' level.

The controller 1501A outputs the selected data 203c as the PCM format data POL when the count result COUNT has 'L' level. On the other hand, the controller 1501A does not output the original selected data 203c as the PCM format data POL when the count result COUNT has 'H' level. At this time, the controller 1501A conducts whether outputting the PCM format data POL which is very small or stopping outputting the PCM format data POL.

According to the fourth limiter 1402, the upper limit value and the lower limit value can be set up, individually and freely. Therefore, the user can obtain the analog voice signal which has a desired band.

Next, the fifth limiter 1402 will be described with Fig. 16 as follows. The fifth limiter 1402 comprises a numerical value data selector 301, a code data selector 302, a comparator 303 and an output portion 1601. The output portion 1601 comprises a logic product (AND gate) 304A, a selector 304B, a code combiner 304C and a controller 1601A. The fifth limiter 1402 has an upper limit value of which format is the absolute value. The upper limit value is calculated by the threshold value setting portion 601.

The code combiner 304C combines the selection result 304b with the code

data of the PCM format data PO and outputs one as the combined data 304c.

The controller 1601A outputs the combined data 304c as the PCM format data POL when the count result COUNT has 'L' level. On the other hand, the controller 1601A does not output the original combined data 304c as the PCM format data POL when the count result COUNT has 'H' level. At this time, the controller 1601A conducts whether outputting the PCM format data POL which is very small or stopping outputting the PCM format data POL.

According to the fifth limiter 1402, the upper limit value and the lower limit value of the fourth limiter can be combined as one limit value. Therefore, the fifth limiter 1402 can save the capacitance of the memory which stores the limit value.

Next, the sixth limiter 1402 will be described with Fig. 17 as follows. The sixth limiter 1402 comprises a numerical value data selector 301, a code data selector 302, a comparator 303 and an output portion 1701. The output portion 1701 comprises a logic product (AND gate) 304A, a code combiner 401A, a selector 401B and a controller 1701A. An upper limit value is calculated by the threshold value setting portion 601.

The selector 401B selects the combined data 401a when the logic product result 304a has 'H' level and outputs one as the selected data 401b. Furthermore, the selector 401B selects the PCM format data PO when the logic product result 304a has 'L' level and outputs one as the selected data 401b.

The controller 1701A outputs the selected data 401b as the PCM format data POL when the count result COUNT has 'L' level. On the other hand, the controller 1701A does not output the original selected data 401b as the PCM format data POL when the count result COUNT has 'H' level. At this time, the controller 1701A conducts whether outputting the PCM format data POL which is very small or stopping outputting the PCM format data POL.

According to the sixth limiter 1402, the original PCM format data PO can be output as the PCM format data POL. Therefore, the sixth limiter 1402 can save the time and power dissipation to combine the numerical value data of the PCM format data PO with the code data again.

Next, the operation of the decoding apparatus with the fourth limiter 1402 according to the fourth preferred embodiment of the present invention will be described with Fig. 18 as follows. As shown in Fig. 18, the decoding apparatus according the fourth preferred embodiment demodulates the receive signals at timing t1, t2, t3, t4,... In this case, the demodulation signal RD at timing t2 has transmission errors. In timing t2, the voltage level of the detection result CRCERR is 'H' level.

Until the point 1801 from the point 1800, the PCM format data PO decoded by the ADPCM decoder 102, is lower than the upper limit value and higher than the lower limit value. The limiter 1402 outputs the PCM format data PO as the

PCM format data POL. Therefore, the PCM decoder 105 decodes the PCM format data PO and outputs the decoded PCM format data AVD.

At the point 1801, the PCM format data PO is lower than the lower limit value. The limit value at this time is the average value which is calculated in the threshold value setting portion 601 based on N data of the PCM format data PO before the point 1801. The limiter 1402 outputs the lower limit value as the PCM format data POL. Therefore, the PCM decoder 105 does not decode the PCM format data PO but the lower limit value, and outputs the decoded lower limit value as the analog voice data AVD. Whenever the PCM format data PO is higher than the upper limit value or lower than the lower limit value, the counter 1401 conducts an increment operation of the count by ones. It goes without saying that the counter 1401 conducts a decrement operation of the count by ones instead of the increment operation.

Until the point 1802 from the point 1801, the PCM format data PO is lower than the upper limit value and higher than the lower limit value. The limit value at this time is the average value which is calculated in the threshold value setting portion 601 based on N data of the PCM format data PO before each point. Therefore, the PCM decoder 105 decodes the PCM format data PO and outputs the decoded PCM format data PO as the analog voice data AVD.

At the point 1802, the PCM format data PO is higher than the upper limit

value. The limit value at this time is the average value which is calculated in the threshold value setting portion 601 based on N data of the PCM format data PO before the point 1802. The limiter 104 outputs the upper limit value as the PCM format data POL. Therefore, the PCM decoder 105 does not decode the PCM format data PO but the upper limit value, and outputs the decoded upper limit value as the analog voice data AVD. The counter 1401 conducts an increment operation of the count by ones. Since then, the decoding apparatus conducts the same operation described the above.

At the point 1805, the limiter 1402 receives the count result COUNT has 'H' level. Until the point 1806 from the point 1805 (term A), the limiter 1402 conducts whether outputting the PCM format data POL which is very small or stopping outputting the PCM format data POL.

The decoding apparatus according to the fourth preferred embodiment of the present invention can have the same effects being described in the first and second preferred embodiments of the present invention.

Furthermore, the decoding apparatus according to the fourth preferred embodiment of the present invention can have the following effect.

The decoding apparatus according to the fourth preferred embodiment of the present invention does not output the PCM format data PO when the total number, the PCM format data PO is over the limit value THV, exceeds the predetermined

